

TINCH-POUND

MIL-S-19500/493A(ER)
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SUPERSEDING
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MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, PNP, THYRISTOR, SILICON, (PROGRAMMABLE UNIJUNCTION TRANSISTOR),
TYPES: 2N6116, 2N6117, 2N6118, 2N6137, 2N6138, JAN, JANTX, AND JANTXV

This specification is approved for use by the Department of the Army and is
available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for PNP, thyristor silicon,
(programmable unijunction transistor). Three levels of product assurance are provided for each
device type as specified in MIL-S-19500.

1.2 Physical dimensions. See figure 1 (T0-18).

1.3 Maximum ratings.

Device types	P_T $T_A = +25^\circ\text{C}$ <u>1/</u>	I_T	I_{TSM} PEAK <u>2/</u>	V_{GKS} <u>3/</u>	V_{GKR}	V_{GAR}	V_{AKR}	V_{AKF}	T_{STG}	T_{OP}
	<u>W</u>	<u>mA (rms)</u>	<u>A dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>°C</u>	<u>°C</u>
2N6116	.300	300	5	40	5	40	40	40	-65	-55
2N6117	.300	300	5	40	5	40	40	40	to	to
2N6118	.300	300	5	40	5	40	40	40	+150	+125
2N6137	.300	300	5	40	5	40	40	40		
2N6138	.300	300	5	100	5	100	100	100		

1/ Derate linearly 2.5 mW/°C for T_A above +25°C.

2/ 10 μs , square wave, 1 percent duty cycle.

3/ Anode shorted to gate.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may
be of use in improving this document should be addressed to: U.S. Army Laboratory Command,
ATTN: SLCET-R-S, Fort Monmouth, NJ 07703-5302 by using the self-addressed Standardization
Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

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FSC 5961

1.4 Primary electrical characteristics.

Device types	I _p V _S = 10 V dc		I _y V _S = 10 V dc			V _F V _S = 10 V dc I _F = 50 mA dc	V _O	I _{GAO} V _{GAO} = 40 V dc V _{GAO} = 100 V dc	
	R _G = 10 kΩ	R _G = 1 MΩ	R _G = 200Ω	R _G = 10 kΩ	R _G = 1 MΩ				
	Max μA dc	Max μA dc	Min mA dc	Min μA dc	Max μA dc	Min V dc	Min V (pk)	Max nA dc	Max nA dc
2N6116	5.0	2.0	---	70	50	1.5	6.0	5	---
2N6117	2.0	0.3	---	50	50	1.5	6.0	5	---
2N6118	1.0	0.15	---	50	25	1.5	6.0	5	---
2N6137	5.0	2.0	1.5	70	50	1.0	9.0	10	---
2N6138	5.0	2.0	1.5	70	50	1.0	9.0	---	10

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.

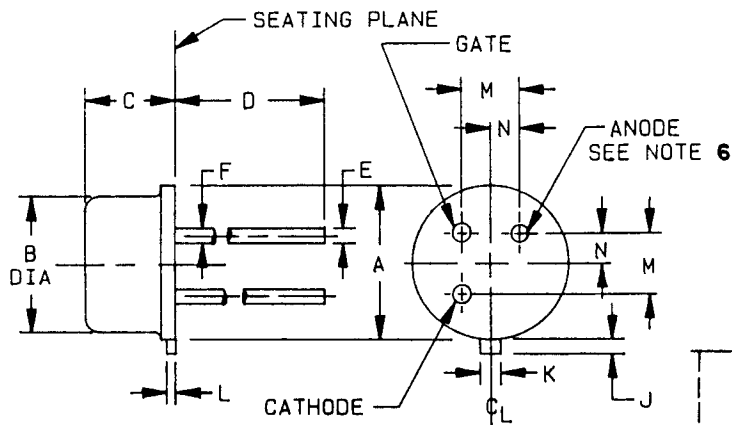
STANDARD

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Dimensions					
Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.209	.230	5.31	5.84	
B	.178	.195	4.52	4.95	
C	.170	.210	4.32	5.33	
D	.500	.750	12.70	19.05	7
E	.016	.021	0.41	0.53	2, 7
F	.016	.019	0.41	0.48	3, 7
J	.028	.048	0.71	1.22	6
K	.036	.046	0.91	1.17	
L	---	.020	---	0.51	
M	.0707 Nom		1.80 Nom		4
N	.0354 Nom		0.90 Nom		4

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Measured in the zone beyond .250 (6.35 mm) from the seating plane.
4. Measured in the zone .050 (1.27 mm) and .250 (6.35 mm) from the seating plane.
5. When measured in a gauging plane .054 +.001, -.000 (1.37 +0.03, -0.00 mm) below the seating plane of the transistor, maximum diameter leads shall be within .007 (0.18 mm) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance. Figure 2 shows the preferred measurement method.
6. On 2N6116, 2N6117, and 2N6118, the gate is connected to the case. On 2N6137 and 2N6138, the gate is connected to the case.
7. Measured from the maximum diameter of the actual device.
8. All three leads.

ANODE

FIGURE 1. Physical dimensions.

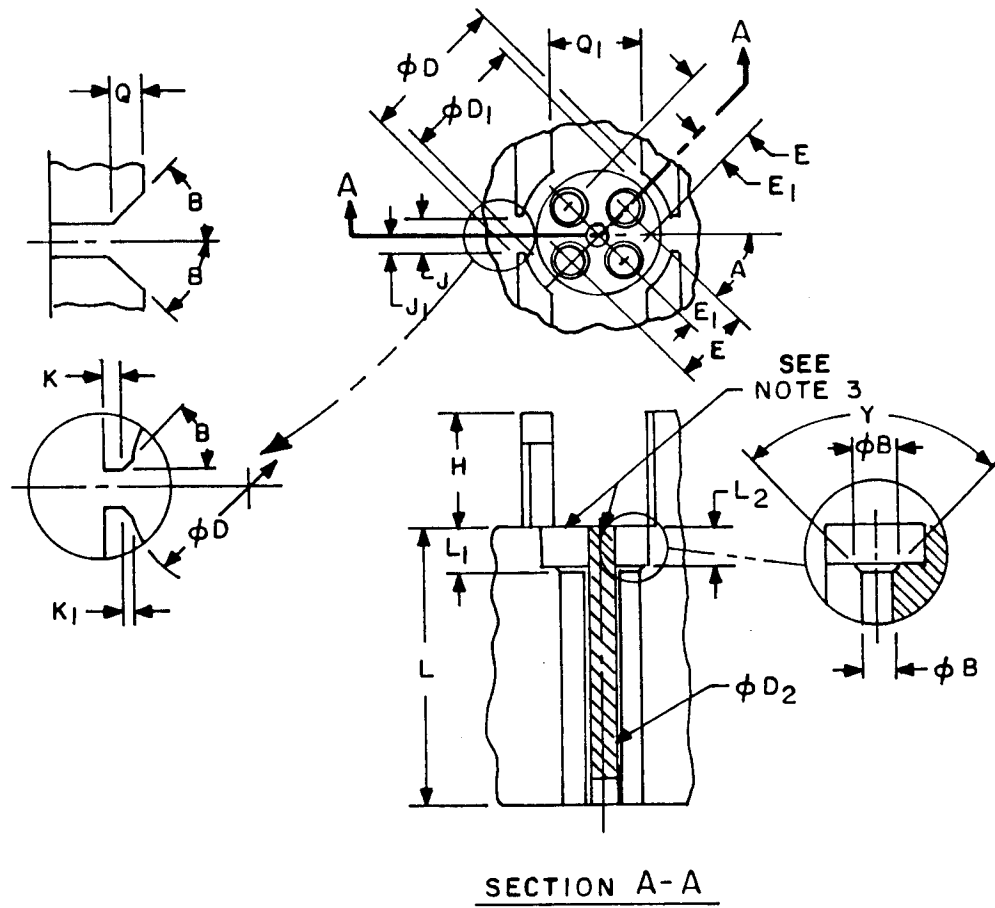


FIGURE 2. Gauge for lead and tab location.

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
ØB	.0325	.0335	0.826	.0851	4
ØB ₁	.043 Nom		1.09 Nom		4
ØD	.2310	.2315	5.867	5.880	
ØD ₁	.159	.161	4.04	4.09	
ØD ₂	.040 Nom		1.02 Nom		5
E	.0995	.1005	2.527	2.553	
E ₁	.0495	.0505	1.257	1.283	
H	.145	.155	3.68	3.94	
J	.0470	.0475	1.194	1.207	
J ₁	.0235	.0245	0.597	0.622	

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
K	.009	.011	0.229	0.279	
K ₁	.005 Nom		0.13 Nom		4
L	.372	.378	9.45	9.60	
L ₁	.054	.055	1.37	1.40	
L ₂	.043 Nom		1.09 Nom		
Q	.040 Nom		1.02 Nom		
Q ₁	.123	.127	3.12	3.23	
A	44.90°		45.10°		
B	45° Nom				
Y	90° Nom				

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. The following gauging procedures shall be used: The device being measured shall be inserted until its seating plane is .125 (3.18 mm) ±.010 (0.25 mm) from the seating surface of the gauge. A force of 8 ±.5 ounces shall then be applied parallel and symmetrical to the device's cylindrical axis. When examined visually after the force application (the force need not be removed) the seating plane of the device shall be seated against the gauge. The use of a pin straightener prior to insertion in the gauge is permissible. A spacer may be used to obtain the .125 (3.18 mm) distance from the gauge seat prior to force application.
4. These surfaces shall be parallel and in same plane within ±.001 (0.03 mm).
5. Four holes.
6. Press in.

FIGURE 2. Gauge for lead and tab location - Continued.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-S-19500.

V_S	- Gate source voltage (see figure 3).
R_G	- Equivalent gate resistance (see figure 4).
I_F	- On-state current, RMS, from anode through cathode (see figure 5).
I_{GAO}	- Gate anode blocking current (dc), cathode (K) open circuited.
I_{GKS}	- Gate to cathode blocking current (dc), anode (A) shorted to gate.
I_P	- Peak point anode current. This is the minimum value of anode current for which the slope of the static anode characteristic curve (see figures 5 and 6) is zero for a specified value of V_S and R_G .
I_T	- Maximum dc forward anode current.
I_{TSM}	- Nonrepetitive peak forward current.
I_V	- Valley point anode current. This is the maximum value of anode current for which the slope of the static anode characteristic curve (see figures 5 and 7) is zero for a specified value of V_S and R_G .
V_{GK}	- Gate to cathode voltage, (dc) voltage from gate (G) to cathode (K).
V_{GA}	- Voltage (dc) from gate (G) to anode (A).
V_{GKR}	- Gate (G) to cathode (K) reverse voltage.
V_{GAR}	- Gate (G) to anode (A) reverse voltage.
V_{AKR}	- Anode to cathode reverse voltage.
V_{AKF}	- Anode to cathode forward voltage.
V_T	- Offset voltage, at the peak point current (I_P). The difference between the anode peak point voltage (V_P) and the gate source voltage (V_S) (see figure 8).
V_F	- On-state voltage. The resultant dc voltage measured between the anode (A) and cathode (K) for specified values of on-state anode current (I_F) (see figure 7).
V_O	- Cathode (K) peak pulse voltage. The cathode peak pulse voltage is defined as shown on figure 9. This parameter is a relative indicator of the peak anode current available for use in firing circuits.
V_P	- Peak point anode voltage. The voltage from anode to cathode when the peak point anode current flows for a specified value of V_S and R_G .
<u>Symbol</u>	- The graphic symbol for the programmable unijunction transistor shall be as shown on figure 10.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-S-19500, and figure 1 herein.

3.3.1 Lead material and finish. Lead material shall be Kovar or Alloy 52; a copper core is permitted. Lead finish shall be gold or tin or solder. Where a choice of lead material or finish is desired, it shall be specified in the contract or purchase order (see 6.2).

3.4 Marking. Marking shall be in accordance with MIL-S-19500. At the option of the manufacturer, the following marking may be omitted from the body of the transistor:

- a. Country of origin.
- b. Manufacturer's identification.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-S-19500.

4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with MIL-S-19500 (table II), and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table II of MIL-S-19500)	Measurement JANTX and JANTXV levels
9	N/A
10	N/A
11	I_{GA0} , I_p , and I_y
12	See 4.3.1
13	ΔI_{GA0} = 50% of initial value or 5 nA dc, whichever is greater; ΔI_p = $\pm 20\%$ of maximum subgroup 2 group A limit. ΔI_y = $\pm 20\%$ of maximum subgroup 2 of group A limit.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:

$T_A = +125^\circ\text{C}$; $I_A = 0$; see figure 11; 2N6116, 2N6117, 2N6118,
 2N6137 = $V_{GK} = 40$ V dc, 2N6138 = $V_{GK} = 100$ V dc.

Note: No heatsink or forced air cooling on the devices shall be permitted.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-S-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-S-19500, and table I herein. (End-point electrical measurements shall be in accordance with the applicable steps of table IV herein.)

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IVb (JAN, JANTX, and JANTXV) of MIL-S-19500, and table II herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table IV herein.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table V of MIL-S-19500, and table III herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table IV herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Forward on-state voltage. The test circuit of figure 7 may be used to measure this parameter. The specified values (see table I) of V_S , R_G and anode current are applied. The anode (A) to cathode (K) voltage is measured as the on-state forward voltage.

4.5.2 Peak point anode current. This parameter shall be measured in the circuit of figure 6 or a suitable equivalent. The variable supply is adjusted to a point just prior to oscillation as detected by the absence of an output voltage pulse. Peak point anode current is the maximum value of I_A just prior to oscillation.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Gate anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}			
2N6116, 2N6117, 2N6118		$V_{GAO} = 40 \text{ V dc}$			5	nA dc
2N6137		$V_{GAO} = 40 \text{ V dc}$			10	nA dc
2N6138		$V_{AOS} = 100 \text{ V dc}$			10	nA dc
Gate cathode blocking current	3036	Bias condition C (see 4.5.6)	I_{GKS}			
2N6116, 2N6117, 2N6118		$V_{GKS} = 40 \text{ V dc}$			50	nA dc
2N6137		$V_{GKS} = 40 \text{ V dc}$			100	nA dc
2N6138		$V_{GKS} = 100 \text{ V dc}$			100	nA dc
Peak point anode current		$V_S = 10 \text{ V dc}$ $R_G = 1 \text{ M}\Omega$ See figure 6 (see 4.5.2)	I_p			
2N6116, 2N6137, 2N6138					2.0	$\mu\text{A dc}$
2N6117					.3	$\mu\text{A dc}$
2N6118					.15	$\mu\text{A dc}$
Peak point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 6 (see 4.5.2)	I_p			
2N6116, 2N6137, 2N6138					5	$\mu\text{A dc}$
2N6117					2	$\mu\text{A dc}$
2N6118					1	$\mu\text{A dc}$
Peak point offset voltage		$V_S = 10 \text{ V dc}$ $R_G = 1 \text{ M}\Omega$ See figure 8 (see 4.5.3)	V_T			
2N6116				.2	1.6	V dc
2N6117, 2N6118, 2N6137, 2N6138				.2	.6	V dc
Peak point offset voltage		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 8 (see 4.5.3)	V_T	.2	.6	V dc

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - continued						
Valley point anode current		$V_S = 10 \text{ V dc}$ $R_G = 1 \text{ M}\Omega$ See figure 7 (see 4.5.4)	I_V			
2N6116, 2N6117, 2N6137, 2N6138 2N6118					50 25	$\mu\text{A dc}$ $\mu\text{A dc}$
Valley point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 7 (see 4.5.4)	I_V			
2N6116, 2N6137, 2N6138 2N6117, 2N6118				70 50		$\mu\text{A dc}$ $\mu\text{A dc}$
Valley point anode current		$V_S = 10 \text{ V dc}$ $R_G = 200\Omega$ See figure 7 (see 4.5.4)	I_V	1.5		mA dc
2N6137, 2N6138 (only)						
Forward on-state voltage		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ $I_F = 50 \text{ mA dc}$ See figure 7 (see 4.5.1)	V_F			
2N6116, 2N6117, 2N6118 2N6137, 2N6138					1.5 1.0	V dc V dc
<u>Subgroup 3</u>						
Low temperature operation		$T_A = -55^\circ\text{C}$				
Peak point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 6 (see 4.5.2)	I_P	.001	10	$\mu\text{A dc}$
High temperature operation:		$T_A = +125^\circ\text{C}$				
Gate anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}		0.5	nA dc
2N6116, 2N6117, 2N6118, 2N6137 2N6138		$V_{GAO} = 40 \text{ V dc}$ $V_{GAO} = 100 \text{ V dc}$				

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - continued						
Valley point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 7 (see 4.5.4)	I_V			
2N6116, 2N6137, 2N6138				40		$\mu\text{A dc}$
2N6117, 2N6118				10		$\mu\text{A dc}$
<u>Subgroup 4</u>						
Peak pulse voltage		See figure 9 (see 4.5.7)	V_0			
2N6116, 2N6117, 2N6118				6.0		V dc
2N6137, 2N6138				9.0		V dc
Peak pulse voltage rise time		See figure 9 (see 4.5.7)	t_r		80	ns
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sample plan, see MIL-S-19500.

TABLE II. Group B inspection for JAN, JANTX, and JANTXV devices.

Inspection <u>1/</u>	MIL-STD-750	
	Method	Conditions
<u>Subgroup 1</u> <u>2/</u>		
Solderability	2026	
Resistance to solvents	1022	
<u>Subgroup 2</u>		
Thermal shock (temperature cycling)	1051	
Hermetic seal Fine leak Gross leak	1071	
Electrical measurements		See table IV steps 1, 3, and 5
<u>Subgroup 3</u>		
Steady-state operation	1027	$T_A = +125^\circ\text{C}$; $I_A = 0$; See figure 11
2N6116, 2N6117, 2N6118, 2N6137 2N6138		$V_{GK} = 40 \text{ V dc}$ $V_{GK} = 100 \text{ V dc}$ No heat sink or forced air cooling on the devices shall be permitted.
Electrical measurements		See table IV steps 2, 4, and 6
<u>Subgroup 4</u>		
Decap internal visual (design verification)	2075	
Bond strength	2037	Test condition A; All internal leads for each device shall be pulled separately.
<u>Subgroup 5</u>		
Not applicable		
<u>Subgroup 6</u>		
High-temperature life (nonoperating)	1032	$T_{STG} = +150^\circ\text{C}$
Electrical measurements		See table IV steps 2, 4, and 6
<u>Subgroup 7</u>		
Not applicable		

1/ For sample plan, see MIL-S-19500.

2/ Separate samples may be used for each test.

TABLE III. Group C inspection (all quality levels).

Inspection <u>1/</u>	MIL-STD-750	
	Method	Conditions
<u>Subgroup 1</u>		
Physical dimensions	2066	See figure 1
<u>Subgroup 2</u>		
Thermal shock (glass strain)	1056	
Terminal strength (tension)	2036	Test condition E
Hermetic seal Fine leak Gross leak	1071	
Moisture resistance	1021	
Electrical measurements		See table IV steps 1, 3, and 5
<u>Subgroup 3</u>		
Shock	2016	
Vibration, variable frequency	2056	
Constant acceleration	2006	
Electrical measurements		See table IV steps 1, 3, and 5
<u>Subgroup 4</u>		
Salt atmosphere (corrosion)	1041	
<u>Subgroup 5</u>		
Not applicable		

See footnotes at end of table.

TABLE III. Group C inspection (all quality levels) - Continued.

Inspection <u>1/</u>	MIL-STD-750	
	Method	Conditions
<u>Subgroup 6</u>		
Steady-state operation life	1026	$T_A = +125^{\circ}\text{C}$ $I_A = 0$ See figure 11
2N6116, 2N6117, 2N6118, 2N6137 2N6138		$V_{GK} = 40 \text{ V dc}$ $V_{GK} = 100 \text{ V dc}$
Electrical measurements		See table IV steps 2, 4, and 6
<u>Subgroup 7 2/</u>		
Capacitive discharge energy $E = 1/2 \text{ CV}^2$		$E = 250 \mu\text{J}$ See figure 12 (see 4.5.8)
Peak anode current		Pulse width = $10 \mu\text{s}$ Duty cycle = 1% Duration = 1 minute See figure 13 (see 4.5.9)
Electrical measurements		See table IV steps 1, 3, and 5

1/ For sample plan, see MIL-S-19500.

2/ Separate samples may be used for each test.

TABLE IV. Groups A, B, and C electrical measurements.

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1	Gate, anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}			
	2N6116, 2N6117, 2N6118		$V_{GAO} = 40 \text{ V dc}$			5	nA dc
	2N6137		$V_{GAO} = 40 \text{ V dc}$			10	nA dc
	2N6138		$V_{GAO} = 100 \text{ V dc}$			10	nA dc
2	Gate, anode blocking current	3036	Bias condition D (see 4.5.5)	I_{GAO}			
	2N6116, 2N6117, 2N6118		$V_{GAO} = 40 \text{ V dc}$			1	$\mu\text{A dc}$
	2N6137		$V_{GAO} = 40 \text{ V dc}$			1	$\mu\text{A dc}$
	2N6138		$V_{GAO} = 100 \text{ V dc}$			1	$\mu\text{A dc}$
3	Peak point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 6 (see 4.5.2)	I_p			
	2N6116, 2N6137, 2N6138					5.0	$\mu\text{A dc}$
	2N6117					2.0	$\mu\text{A dc}$
	2N6118					1.0	$\mu\text{A dc}$
4	Peak point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 6 (see 4.5.2)	I_p	.001		
	2N6116, 2N6137, 2N6138					6.0	$\mu\text{A dc}$
	2N6117					3.0	$\mu\text{A dc}$
	2N6118					2.0	$\mu\text{A dc}$
5	Valley point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 7 (see 4.5.4)	I_v			
	2N6116, 2N6137, 2N6138				70		$\mu\text{A dc}$
	2N6117, 2N6118				50		$\mu\text{A dc}$
6	Valley point anode current		$V_S = 10 \text{ V dc}$ $R_G = 10 \text{ k}\Omega$ See figure 7 (see 4.5.4)	I_v			
	2N6116, 2N6137, 2N6138				55		$\mu\text{A dc}$
	2N6117, 2N6118				35		$\mu\text{A dc}$

4.5.3 Peak point offset voltage. This parameter shall be measured in the circuit of figure 8. The peak point offset voltage is equal to the peak point anode voltage minus the gate source voltage (V_S), immediately prior to triggering.

4.5.4 Valley point anode current. For the specified gate supply voltage (V_S) (see table I) and gate source resistance (R_G), the anode current corresponding to the valley point operating condition is measured. The test circuit of figure 7 or suitable equivalent, shall be used for this measurement. The specified gate supply voltage (V_S) and gate source resistance (R_G) shall be applied. The bias voltage shall be gradually increased until the device fires and then shall be varied to obtain a minimum value of V_{AK} . The I_A corresponding to this minimum value of V_{AK} is the I_V of the device under test.

4.5.5 Gate anode blocking current. This test shall be conducted in accordance with method 3036 of MIL-STD-750 except that the words and symbols, collector (C), base (B), and emitter (E) shall be replaced with gate (G), anode (A), and cathode (K), respectively.

4.5.6 Gate cathode blocking current. This test shall be conducted in accordance with method 3036 of MIL-STD-750, except that the words and symbols, collector (C), base (B) and emitter (E) shall be replaced with gate (G), anode (A), and cathode (K) respectively.

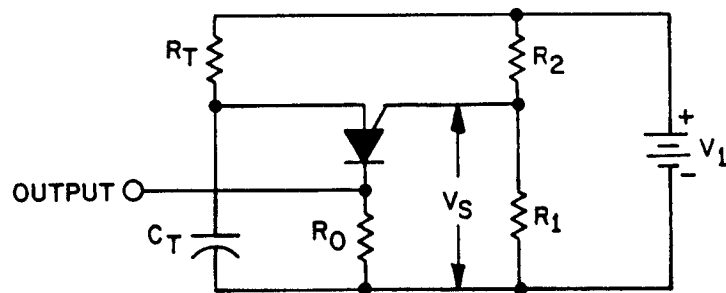
4.5.7 Cathode peak pulse voltage. This test shall be conducted in the circuit of figure 9. The peak pulse voltage (V_G) is observed by an oscilloscope across the 20Ω resistor. The rise time of the pulse is defined as the time for the waveform to rise from 0.6 V to 6 V.

4.5.8 Capacitive discharge energy. The test shall be conducted in the circuit of figure 12. The CDE in micro joules is to be calculated from $E = 1/2 CV^2$. The circuit shall be allowed to cycle a minimum of five times. The total test time shall be approximately 1 minute.

4.5.9 Peak anode current. This test shall be conducted in the circuit of figure 13. Adjust R_a for 5 V peak on oscilloscope. The total test time shall be a minimum of 1 minute duration.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-S-19500.



$$V_S = R_1(V_1/R_1 + R_2)$$

FIGURE 3. Typical oscillator circuit.

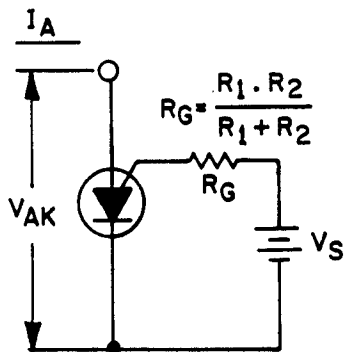


FIGURE 4. Equivalent test circuit used for electrical characteristics testing.

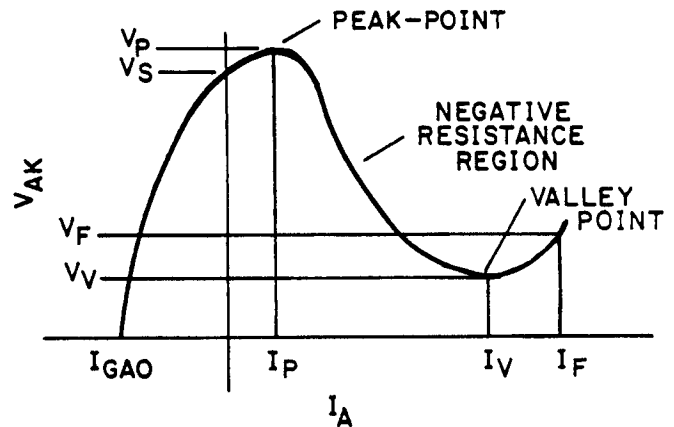
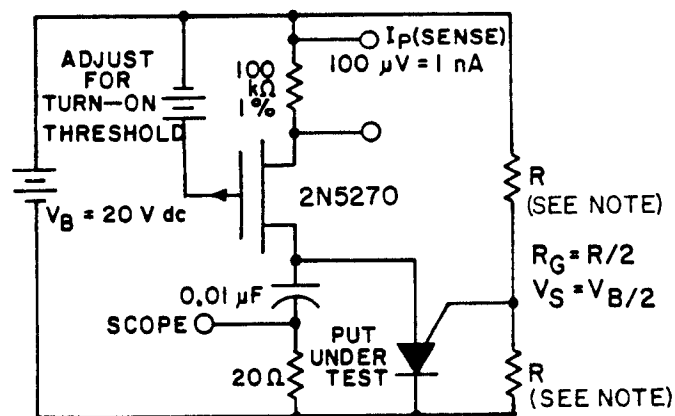
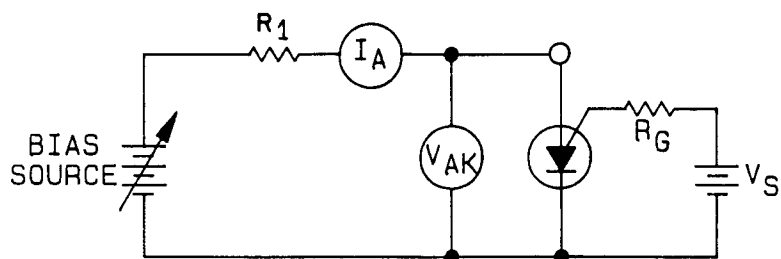


FIGURE 5. Static characteristics.



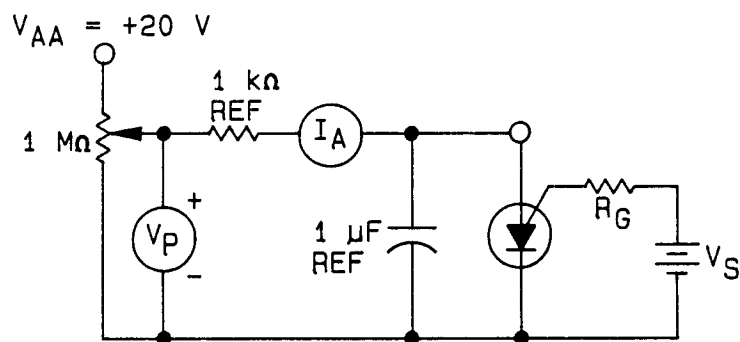
NOTE: Use 1 percent metal film resistors.

FIGURE 6. Peak current (I_P) test circuit.



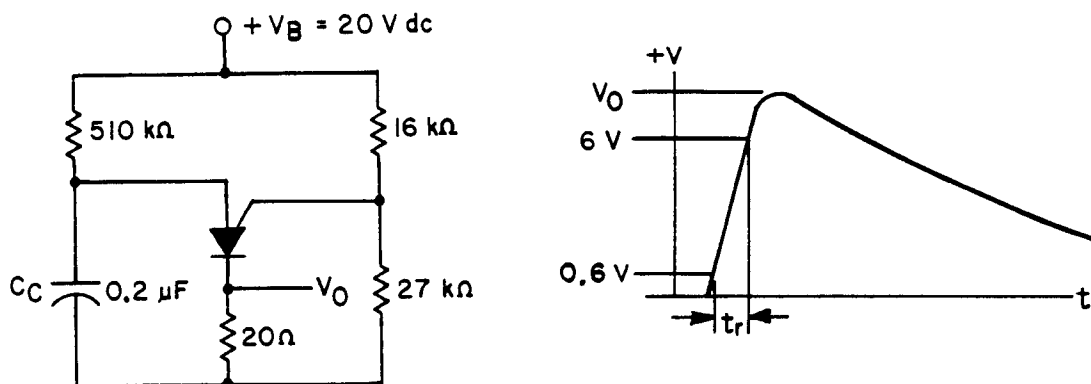
NOTES:

1. R_1 chosen to limit current to a safe value.
2. Bias source is a well regulated 1 mV peak to peak ripple supply.

FIGURE 7. Valley point anode current and forward on-state voltage circuit.

NOTES:

1. 1 MΩ pot must be noiseless to prevent false triggering.
2. Voltage source with less than 1 mV peak to peak ripple.

FIGURE 8. Offset voltage circuit.FIGURE 9. V_0 and t_r test circuit.

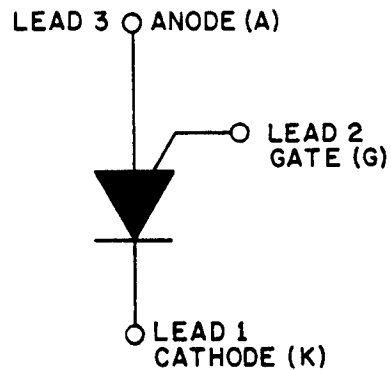
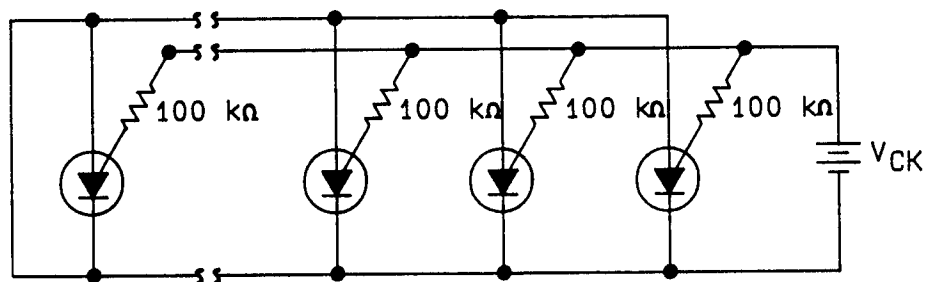


FIGURE 10. Symbol for programmable unijunction transistor.



NOTE: Any number of devices under test may be added in parallel up to the maximum capability of the power supply to maintain voltage under the theoretical worst case condition if all devices under test shorted.

FIGURE 11. Burn-in and operating life test circuit.

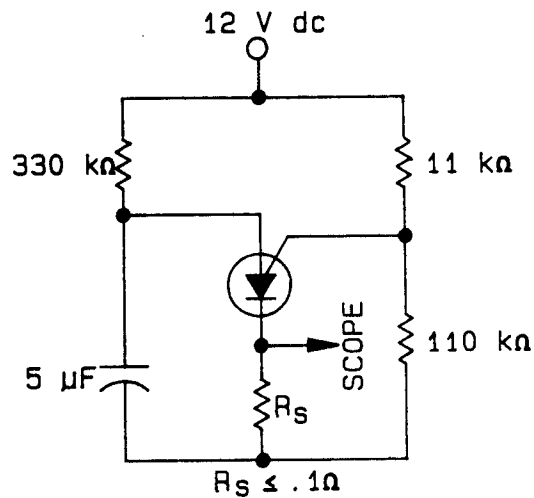
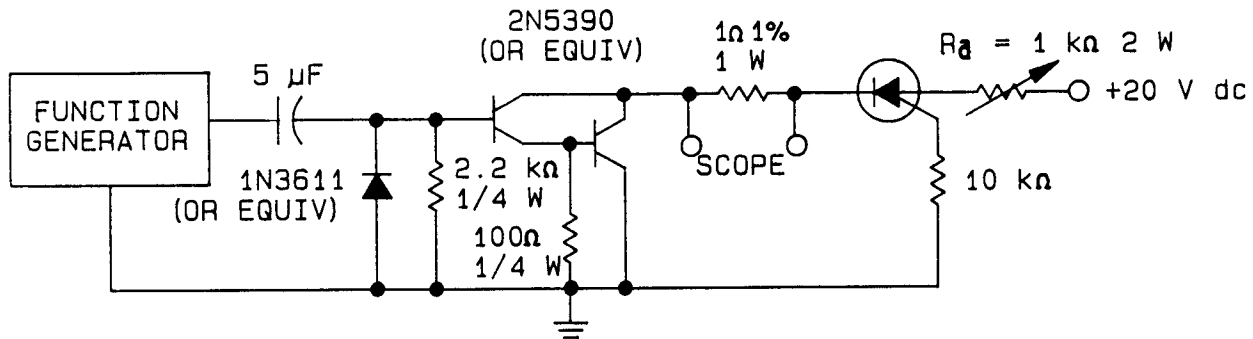


FIGURE 12. Capacitive discharge energy test circuit.



NOTE: Adjust function generator to pulse width = 10 μ s (square wave) and repetition rate = 1 kHz. Adjust R_a for 5 V peak (equivalent to 5 A peak). Total test time = 1 minute minimum.

FIGURE 13. Peak anode current test circuit.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

6.2 Ordering data. Acquisition documents may specify the lead material and finish (see 3.3.1).

6.3 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's part number. This information in no way implies that manufacturer's part numbers are suitable as a substitute for the Part or Identifying Number (PIN). The term PIN is equivalent to the term (part number, identification number, and type designator) which was previously used in this specification.

PIN	Manufacturer's CAGE code	Manufacturer's and user's part number

CONCLUDING MATERIAL

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Army - ER

Preparing activity:
Army - ER

Agent:
DLA - ES

(Project 5961-A973)

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MIL-S-19500/493A(ER)

2. DOCUMENT TITLE

Semiconductor Device, PNP, Thyristor, Silicon, Types 2N6116-18

3a. NAME OF SUBMITTING ORGANIZATION**4. TYPE OF ORGANIZATION (Mark one)**

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